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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,711	11/12/2003	Shridhar Mukund	ADAPP222	9276

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EXAMINER	
LO, SUZANNE	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 11/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,711	MUKUND ET AL.	
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. **Claims 1-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimogori et al. (U.S. Patent Application No. 2002/0152061A1) **in view of Shridhar et al. (U.S. Patent No. 5,815,714).**

As per claim 1, Shimogori is directed to a method for simulating a chip circuit **([0053])**, comprising: defining a library of components for a processor **([0082]-[0083])**; defining interconnections for a set of pipelined processors including the processor **([0047])**, *the interconnections defined by*

analyzing the architectural representation of adjacent processors **([0047]-[0048])**; generating a processor circuit by combining the library of components and the interconnections for the set of pipelined processors **([0083])**; generating a code representation of a model of the set of pipelined processors **([0058])**; and comparing signals generated by the code representation to signals generated by the processor circuit **([0062])**, wherein if the comparison of the signals is unacceptable, the method includes, identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit **([0090])** but fails to explicitly disclose *generating output for display to identify a cause of the unacceptable comparison of the signals at a block level of the processor circuit.*

Shridhar teaches inserting a print command to determine the signal level location of an error **(column 4, lines 40-42)**. Shimogori and Shridhar are analogous art because they are from the same field of endeavor, testing and debugging code. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the chip circuit simulation method of Shimogori with the debugging print commands of Shridhar in order to provide convenient means for modifying the underlying source code as required **(Shridhar, column 3, lines 44-47)**.

As per claim 2, the combination of Shimogori and Shridhar already discloses the method of claim 1, wherein the library of components is included as register transfer logic (RTL) **(Shimogori, [0053])**.

As per claim 3, the combination of Shimogori and Shridhar already discloses the method of claim 1, wherein the interconnections for the set of pipelined processors is included in a structural netlist **(Shimogori, [0099])**.

As per claim 4, the combination of Shimogori and Shridhar already discloses the method of claim 1, wherein the set of pipelined processors are configured to manipulate layers of a header of a data packet in stages **(Shimogori, [0068])**.

As per claim 5, the combination of Shimogori and Shridhar already discloses the method of claim 1, wherein the method operation of identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes, inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals **(Shimogori, [0091])**.

As per claim 6, the combination of Shimogori and Shridhar already discloses a method for debugging a processor circuit, comprising: identifying a block level location having an error from a first simulation **(Shimogori, [0090])**; inserting a patch into a thread specific to the block level location of the error **(Shimogori, [0091])**; executing the simulation to determine a signal level location of the error through information generated by the patch **(Shimogori, [0091])**; and correcting a code representation of a processor associated with the error **(Shimogori, [0093])**.

As per claim 7, the combination of Shimogori and Shridhar already discloses the method of claim 6, wherein the patch is a print command **(Shridhar, column 4, lines 40-42)**.

As per claim 8, the combination of Shimogori and Shridhar already discloses the method of claim 6, wherein the method operation of executing the simulation to determine a signal level location through information generated by the patch includes, triggering a print statement indicating the signal level location of the error **(Shridhar, column 4, lines 40-42)**.

As per claim 9, Shimogori is directed to an apparatus for simulating a chip circuit **([0053])**, comprising: *a server in which a simulation program logic is stored, the server configured to execute the simulation program logic* **([0018])**, *wherein the simulation program logic includes:* logic for generating a processor circuit by combining a library of components and defined interconnections for a set of pipelined processors **([0082]-[0083], [0047])** *the interconnections defined by analyzing the architectural representation of adjacent processors* **([0047]-[0048])**; logic for generating a code representation of a model of the processor **([0058])**; and logic for comparing signals generated by the code representation to

signals generated by the processor circuit **([0062])**, wherein if the comparison of the signals is unacceptable, the logic for comparing signals includes, logic for identifying a cause of the unacceptable comparison of the signals at a block level of the code representation **([0090])** but fails to explicitly disclose *generating output for display to identify a cause of the unacceptable comparison of the signals at a block level of the code representation.*

Shridhar teaches inserting a print command to determine the signal level location of an error **(column 4, lines 40-42)**. Shimogori and Shridhar are analogous art because they are from the same field of endeavor, testing and debugging code. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the chip circuit simulation method of Shimogori with the debugging print commands of Shridhar in order to provide convenient means for modifying the underlying source code as required **(Shridhar, column 3, lines 44-47)**.

As per claim 10, the combination of Shimogori and Shridhar already discloses the apparatus of claim 9, wherein logic for identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes, logic for inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals **(Shimogori, [0091])**.

As per claim 11, the combination of Shimogori and Shridhar already discloses the apparatus of claim 9, wherein the library of components is included as register transfer logic (RTL) **(Shimogori, [0053])**.

As per claim 12, the combination of Shimogori and Shridhar already discloses the apparatus of claim 9, wherein the interconnections for the set of pipelined processors is included in a structural netlist **(Shimogori, [0099])**.

As per claim 13, the combination of Shimogori and Shridhar already discloses the apparatus of claim 10, wherein the patch includes logic for executing a print statement **(Shridhar, column 4, lines 40-42)**.

As per claim 14, the combination of Shimogori and Shridhar already discloses the apparatus of claim 9, wherein each logic component is one of hardware and software **(Shimogori, [0101])**.

As per claim 15, Shimogori is directed to a computer readable medium **([0101])** *in which* program instructions *are stored, the program instructions when read by a server of a computing system* **([0018])**, *cause the server to perform a method* for simulating *a model of a* chip circuit, *the method* comprising: defining a library of components for a processor **([0082]-[0083])**; defining interconnections for a set of pipelined processors including the processor **([0047])**, *the interconnections defined by analyzing the architectural representation of adjacent processors*; generating a processor circuit by combining the library of components and the interconnections for the set of pipelined processors **([0083])**; generating a code representation of a model of the set of pipelined processors **([0058])**; and comparing signals generated by the code representation to signals generated by the processor circuit **([0062])**, wherein if the comparison of the signals is unacceptable, the *method* includes, identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit **([0090])** but fails to explicitly disclose *generating output for display to identify a cause of the unacceptable comparison of the signals at a block level of the processor circuit.*

Shridhar teaches inserting a print command to determine the signal level location of an error **(column 4, lines 40-42)**. Shimogori and Shridhar are analogous art because they are from the same field of endeavor, testing and debugging code. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the chip circuit simulation method of Shimogori with the debugging print commands of Shridhar in order to provide convenient means for modifying the underlying source code as required **(Shridhar, column 3, lines 44-47)**.

As per claim 16, the combination of Shimogori and Shridhar already discloses the computer readable medium of claim 15, wherein the library of components is included as register transfer logic (RTL) **(Shimogori, [0053])**.

As per claim 17, the combination of Shimogori and Shridhar already discloses the computer readable medium of claim 15, wherein the interconnections for the set of pipelined processors are included in a structural netlist **(Shimogori, [0099])**.

As per claim 18, the combination of Shimogori and Shridhar already discloses the computer readable medium of claim 15, wherein the set of pipelined processors are configured to manipulate layers of a header of a data packet in stages **(Shimogori, [0068])**.

As per claim 19, the combination of Shimogori and Shridhar already discloses the computer readable medium of claim 15, wherein identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit includes, program instructions for inserting a patch into the code representation to identify a signal level location for the unacceptable comparison of the signals **(Shimogori, [0091])**.

Response to Arguments

3. The 35 U.S.C. 112, 2nd paragraph rejections of claims 5, 10, 19 and the 35 U.S.C. 101 rejections of claims 1-8 and 15-19 are withdrawn due to the amended claims.

4. Applicant's arguments filed 09/21/06 have been fully considered but they are not persuasive.

5. Claims 9-14 are still rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Specifically, claims 9-14 are directed to software, *per se*, which is abstract. Claims 9-14 are written so broadly they need not include hardware, only software as the server as stated by claim 9 may be a process as opposed to a computer.

6. The Applicant makes the argument that the library of instruction sets of Shimogori does not disclose the library of components that is claimed in the claimed invention. The Applicant is directed to

paragraphs **[0030]-[0031]** where the *"special-purpose instruction library may be converted into RTL before another ISS simulation is performed"* and as such Shimogori clearly teaches that the library of instruction sets are instructions for components of a chip circuit. If the library of instruction sets for circuit components of Shimogori is different from the library of components of the claimed invention, the Examiner respectfully requests that the Applicant explain how the library of components claimed in the instant application is enabled without "instruction sets" or code. The Examiner also respectfully requests that the Applicants identify support for such an enablement in the instant application.

In response to Applicant's argument that Shimogori does not disclose a plurality of processors, the Applicant is further directed to **Figure 1, VU 1** and **PU 2** as well as paragraph **[0046]**. With a general-purpose data processing unit (VU) and a special-purpose processing unit (PU), Shimogori discloses a plurality of processors with interconnections.

In response to Applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., where each of the plurality of processors are equipped with input socket interface, star processor, output socket interface, etc....) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to Applicant's argument that Shimogori does not suggest or teach comparison of signals, Applicant is further directed to paragraph **[0067]** where *"pseudo-VU instructions provide processing that inputs data into the ISS system or outputs expected values in order to evaluate the progress or result of the simulation"* where the expected values are derived from *"an actual processor (which) also handles such instructions as pseudo-VU instructions"*. Examiner also directs the Applicant to paragraph **[0062]** where *"bit pattern from a signal stream"* clearly discloses signals generated by a processor circuit or signals generated by code representation of the processor circuit.

In response to Applicant's argument that Shimogori does not suggest or teach identifying a cause of the unacceptable comparison of the signals at a block level of the processor circuit, the Examiner first notes that Shimogori does indeed teach signal generation and signal comparison as cited above. Furthermore, Applicant is directed to **[0090]** where parts of the code can be sped up. If there are too many cycles that are consumed by the VU instructions then the bit patterns of the generated signals from the simulated processor will not match and cause an unacceptable comparison with the expected signals. As Shimogori identifies which parts of the code can be speeded up, Shimogori identifies causes of unacceptable comparison of the signals at a block level of the code representation.

The Applicant also makes argument that Shimogori does not suggest or teach identifying a cause of the unacceptable comparison of signals at a block level of the processor circuit as suggested by the claimed invention because Shimogori does not mention any block level processing. As shown in paragraphs **[0006]-[0007]** of the specification of the instant application, the "block level" simulation is modeled in the method of **Figure 1** of the instant application where indeed the components are modeled as blocks, therefore the processing between the blocks are block level modeling. Shimogori teaches the same, as shown in **Figure 1** of Shimogori. Although Shimogori does not explicitly state, "block level processing", it is apparent to one of ordinary skill in the art of processor design that Shimogori is directed to block level processing as all components are represented and modeled as blocks. As Shimogori clearly models components on a block level, the Examiner respectfully requests that the Applicant explain how the block diagrams as well as simulation of block level processing of Shimogori and the instant application are different.

In regards to claim 6, Applicant is directed to the previous argument made of comparing signals and identifying a cause for unacceptable comparison of signals. As Shimogori identifies a cause of an unacceptable comparison of signals – a cause of too many cycles – by definition, Shimogori identifies an error (**[0062]**). Also, as Shimogori includes code which will eliminate the cause of unacceptable

comparison of signals – which will increase the speed of execution and reduce the number of cycles to an acceptable number – Shimogori inserts a patch into a thread specific to the block level location of the error ([0090]).

Conclusion

7. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suzanne Lo
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11/15/06

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